CLAIMS

What is claimed is:

1. A method for calculating a log-likelihood ratio for each bit of a symbol transmitted in a communication system comprising the steps of:

modulating a symbol comprised of one or more bits according to a predetermined mapping scheme having corresponding characteristics;

transmitting the modulated symbol to at least one receiver;

receiving the modulated symbol and demodulating the modulated symbol with the at least one receiver; and

calculating a corresponding log-likelihood ratio for each of the one or more bits of the demodulated symbol by eliminating calculation steps used to determine the log-likelihood ratio through predetermined logic conditions based on the corresponding characteristics of the predetermined mapping scheme.

2. The method according to claim 1, wherein the predetermined mapping scheme includes a square Karnaugh mapping.

3. The method according to claim 2, wherein the corresponding characteristics of the predetermined mapping scheme include mirror symmetry for a constellation of symbol values about horizontal and vertical axes for all of the one or more bits in each of the symbols in the constellation except for two predetermined bits of each symbol in those symbols having more than two bits, wherein the two predetermined bits have opposing values for symbols on respective opposing sides of the horizontal and vertical axes.

4. The method according to claim 3, wherein for each of the two predetermined bits, symbols on a side of an axis have the predetermined bit set at a first binary value and remaining symbols on another opposing side of the axis have the predetermined significant bit set at a second binary value.

5. The method according to claim 3, wherein the symbol value is formatted as a twos complement having a sign bit, one or more integer bits and one or more fractional bits, and

wherein the predetermined logic conditions include:

a) performing intermediate difference calculations in the directions of the horizontal and vertical axes using the twos complement sign bit, the one or more integer bit and the one or more fractional bits, the difference calculations based on the asymmetric and symmetric characteristics of the symbol bits in the Karnaugh mapped symbol constellation to achieve a plurality of difference values;

b) determining two minimum distances of each bit in the received demodulated symbol to corresponding two closest constellation points of the Karnaugh mapped symbol constellation having corresponding bit values of one and zero, respectively, by selecting one or more of the plurality of difference values based on selection criterion predetermined for each particular bit of the demodulated symbol, the selection criterion based on characteristics of the Karnaugh mapping; and

c) squaring the determined two minimum distances of each bit and taking the difference of the squares to obtain the log-likelihood ratio of each bit of the demodulated symbol.

6. The method according to claim 2, wherein the predetermined mapping scheme further includes Gray coding.

7. The method according to claim 1, wherein the symbol is comprised of $\log_2 M$ bits and is modulated according to a M-ary Quadrature Amplitude Modulation scheme.

8. The method according to claim 7, wherein the M-ary Quadrature Amplitude Modulation scheme has 64 symbols and each symbol is comprised of six bits.

9. An apparatus for determining a log-likelihood ratio for each bit of a demodulated symbol received by a communication system, the apparatus comprising:

a receiver portion configured to receive a demodulated symbol modulated according to an M-ary quadrature amplitude modulation;

a combinatorial logic configured to determine one or more characteristics of the received demodulated symbol;

a plurality of first additive devices each configured to perform a corresponding additive operation of a corresponding value to a portion of the received demodulated symbol and output a corresponding resultant value;

a plurality of multiplexers arranged in pairs, each of the multiplexers configured to receive particular ones of the resultant values from one or more of the plurality of first additive devices, each of the multiplexers outputting one of the input resultant values based on states of the at least one of the one or more characteristics of the received demodulated symbol as determined by the combinatorial logic;

a plurality of squaring blocks arranged in pairs corresponding to the pairs of multiplexers, each of the plurality of squaring blocks connected to a corresponding one the plurality of multiplexers and configured to square the particular resultant output by the corresponding multiplexer; and

a plurality of second additive devices each configured to calculate a difference between outputs of a corresponding arranged pair of the plurality of squaring blocks, wherein the difference represents a log-likelihood ratio for a particular bit of the demodulated symbol.

10. The apparatus according to claim 9, wherein the demodulated symbols were modulated according to a predetermined mapping scheme that includes a square Karnaugh mapping scheme.

11. The apparatus according to claim 10, wherein the additive operations of the plurality of first additive devices are predetermined based on characteristics of the

Karnaugh mapping scheme.

12. The apparatus according to claim 11, wherein the characteristics of the Karnaugh mapping scheme include mirror symmetry for a constellation of symbol values about horizontal and vertical axes for all of the one or more bits in each of the symbols in the constellation except for two predetermined bits of each symbol in those symbols having more than two bits, wherein the two predetermined bits have opposing values for symbols on respective opposing sides of the horizontal and vertical axes.

13. The apparatus according to claim 12,wherein for each of the two predetermined bits, symbols on a side of an axis have the predetermined bit set at a first binary value and remaining symbols on another opposing side of the axis have the predetermined significant bit set at a second binary value..

14. The apparatus according to claim 10, wherein the predetermined mapping scheme further includes Gray coding.

15. The apparatus according to claim 9, wherein the symbol is comprised of a $\log_2 M$ number of bits and is modulated according to a M-ary Quadrature Amplitude Modulation scheme.

16. The apparatus according to claim 15, wherein the M-ary Quadrature Amplitude Modulation scheme has 64 symbols each having 6 bits.

17. The apparatus according to claim 9, wherein the one or more characteristics determined by the combinatorial logic include a sign of the demodulated symbol and positional information of the demodulated symbol relative to axes of a Karnaugh mapped constellation of symbols and also relative to predetermined values on the axes.

18. The apparatus according to claim 9, wherein the plurality of first additive devices are arranged in parallel and have outputs controlled by a first clock;

the plurality of multiplexers are arranged in parallel and have outputs controlled by a second clock; and

the plurality of second additive devices are arranged in parallel and have outputs controlled by a third clock.

19. The apparatus according to claim 9, wherein the demodulated symbol value is formatted as a twos complement having a sign bit, one or more integer bits and one or more fractional bits; and

wherein the receiver portion is configured to separate the symbol value into the sign bit, the one or more integer bits, the one or more fractional bits and derive an absolute value of the symbol.